REMARKS

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested. Since the present Response raises no new issues, and in any event, places the application in better condition for consideration on appeal, entry thereof is respectfully requested under the provisions of 37 C.F.R. § 1.116.

Applicants take this opportunity to address the Examiner's comments in the Response to Arguments portion of the outstanding Final Office Action. Referring to the Page 6 of the Final Office Action, the Examiner states the following:

> "Bronner discloses wordlines and interconnects made of the same material. (For example: See Column 3, lines 44-67)."

Claim 57 requires that at least one wordline and the local interconnect are comprised of identical material. Turning to Column 3, lines 65-67, of Bronner et al., the portion of Bronner et al. being relied upon by the Examiner to meet the above noted limitation recites the following:

> "layers 322, 315, and 310 are etched to define the gates, wordlines (and, optionally, local interconnects) both in the array and outside the array.)".

The Examiner also relies upon Figure 4 for the disclosure of layers 315 and 310 in both the support and the array region of the device, alleging that this disclosure meets the limitation of the wordline and the local interconnect being comprised of identical material, as required by Claim 57.

First, as indicated above, the local interconnect structure is optional in Bronner et al. Further, there is no disclosure of a local interconnect structure in Figure 4, and Bronner et al. does not disclose an interconnect composed of an identical material as a wordline, as required by Applicants' claims. Finally, as previously indicated in the response to the Office Action dated

June 4, 2008, referring to Column 4, lines 1-5, Bronner et al. discloses that the second polysilicon layer 315 is deposited in the array region to produce a uniform gate height between the array and support regions. The height of the first polysilicon layer 310 in the support region remains constant and does not include second polysilicon layer 315, since the height of the first polysilicon layer is not reduced during array processing due to being protected by a masking layer. Therefore, the support region comprises interconnect structures consisting only of first polysilicon layer 310. Therefore, since the array region consists of composite structures 310, 315 and the support region structures consist solely of layer 310; Bronner et al. fails to disclose where at least one wordline and said local interconnect are comprised of identical material.

Applicants note that "it is impermissible within the framework of §103 to pick and choose from any one reference only as much of it as well support a give position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggest to one of ordinary skill in the art". *In re Wesslau,* 147 U.S.P.Q. 391, 393 (1965). Therefore, because the text of the Bronner et al. reference indicates that the local interconnect is not composed of the same material/identical structure as the wordline, and Figure 4 fails to depict a local interconnect, Applicants submit that Bronner et al. fails to disclose where at least one wordline and said local interconnect are comprised of identical material, as required by Claim 57.

Turning to the present grounds of rejection, Claims 57-59 and 62 stand rejected, under 35 U.S.C. §103(a), as allegedly unpatentable over U.S. Patent No. 5,945,704 to Schrems et. al. ("Schrems et al.") in view of U.S. Patent No. 6,174,756 to Gambino et al. ("Gambino et al."), and further in view of U.S. Patent No. 5,525,531 to Bronner et al. ("Bronner et al."). Claims 60 and 61 stand rejected, under 35 U.S.C. §103(a), as allegedly unpatentable over Schrems, et al. in

view of Gambino et al., Bronner et al., and the publication "Microchip Fabrication" by Peter Van Zant ("Peter Van Zant"). Applicants traverse the aforementioned rejections and submit the following.

Applicants submit that the applied references do not fulfill the requirements to support a prima facie case of obviousness with respect to Claim 57. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art". *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970). Applicants submit that the applied prior art fails to render Applicants' invention unpatentable, because the applied prior art fails to teach or suggest a device in which the at least one wordline and said interconnect are comprised of identical material, as recited in Claim 57.

Schrems et al. discloses a structure including only an array region of a device. Schrems et al. does not teach or suggest the limitation of a support region, as recited in Claim 57. Further, Schrems et al. does not teach or suggest at least one support region having a local interconnect formed therein, in which at least one wordline and the local interconnect are comprised of identical material, as recited in Claim 57.

Gambino et al. fails to fulfill the deficiencies of Schrems et al., because Gambino et al. also fails to teach or suggest a local interconnect formed in the support region, where the local interconnect and the wordline of the device are comprised of the same material, as recited in Claim 57.

Gambino et al. discloses a structure having a second region (array region) 130 and a first region 110, where the first region 110 comprises a semiconducting device 115. Gambino et al. discloses where a gate oxide 160 is deposited atop a substrate followed by the deposition of a gate layer 161, which are then patterned forming a gate stack 115 in the first region 110. The

incorporation of the gate oxide 160 into gate stack 115, results in a gate conductor that is not in direct contact with the substrate surface, and is therefore not an interconnect structure. Additionally, Gambino et al., discloses forming source and drain regions 117, 118; further supporting that the gate stack 115 is not an interconnect but a semiconducting device, where the device's conductivity is dependent on the thickness of the gate oxide 160. Since Gambino et al. fails to teach or suggest an interconnect in the support region of the device, Gambino et al. also fails to teach or suggest a structure having a wordline and interconnect, where the wordline and interconnect are comprised of the same material. Therefore, Gambino et al. does not teach or suggest a support region having an interconnect, where the interconnect and wordline are comprised of the same material, as recited in Claim 57.

Bronner et al. also fails to fulfill the deficiencies of the applied references, since this applied reference also fails to teach or suggest a local interconnect formed in the support region and where the local interconnect and wordline of the device comprise an identical material, as recited in Claim 57. It is the Examiner's position in the present Final Office Action, that "Bronner et al. discloses wordlines and interconnects made of the same material (For Example: See Column 3 lines 44-67)." Applicants respectfully disagree and present the following.

Applicants disclose, referring to FIG. 24, where a local interconnect 94 comprising the same materials as the opposing wordline, those structures comprising wordline conductor 54, being W/WN. Referring to the passage of Bronner et al. cited by the Examiner, Column 3, lines 44-67, Bronner et al. discloses where layers "322, 315 and 310 are etched to define the gate, wordlines (and optionally, local interconnects) both in the array and outside it." Layer 322 represents a cap layer; layer 315 represents a second polysilicon layer and layer 310 represents a first polysilicon layer.

Applicants submit that prior to etching layers 322, 315 and 310, Bronner et al. discloses masking the support region and processing the array region, where during array processing the height of the polysilicon layer 310 is reduced. See Bronner, Column 3, lines 44-65. Bronner et al. further discloses that the original height of the first polysilicon layer 310 in the array region is thereafter restored by depositing a second polysilicon layer 315 until the original height of the first polysilicon layer 310 within the array region is restored; resulting a composite gate structure including layers 310, 315.

Applicants observe, referring to Column 4, lines 1-5, that Bronner et al. further discloses that the second polysilicon layer 315 is deposited in the array region to produce a uniform gate height between the array and support regions. The height of the first polysilicon layer 310 in the support region remains constant and does not include second polysilicon layer 315, since the height of the first polysilicon layer is not reduced during array processing due to being protected by the masking. Therefore, the support region comprises gate or interconnect structures consisting only of first polysilicon layer 310. Therefore, since the array region consists of composite structures 310, 315 and the support region structures consist solely of layer 310; Bronner et al. fails to disclose where at least one wordline and said local interconnect are comprised of identical material.

Peter Van Zant also fails to fulfill the deficiencies of the applied references, since this applied reference also fails to teach or suggest a local interconnect formed in the support region and where the local interconnect and wordline of the device are comprised of an identical material, as recited in Claim 57. Peter Van Zant is far removed for Applicant's invention and has only been cited for potential applications of silicon nitride. Peter Van Zant does not teach or

suggest at least one support region having a local interconnect formed therein, where at least one wordline and said interconnect are comprised of identical material, as recited in Claim 57.

Therefore, Applicants submit the present § 103 rejection has been obviated, and respectfully request withdrawal thereof.

Wherefore, consideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,

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